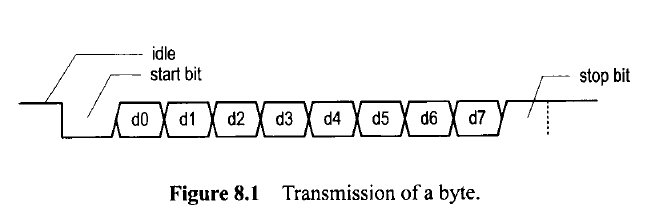
See FPGA prototyping with verilog examples.pdf, chapter 8, page 215



baud rate (i.e., number of bits per second), the number of data bits and stop bits, and use of

the parity bit. The commonly used baud rates are 2400,4800, 9600, and 19,200 bauds.

We use an ***oversampling scheme***

to estimate the middle points of transmitted bits and then retrieve them at these points

accordingly.

The most commonly used sampling rate is 16 times the baud rate, which means that each

serial bit is sampled 16 times

For the 19,200 baud rate, the sampling rate has to be 307,200 (i.e., 19,200\* 16) ticks per

second. Since the system clock rate is 50 MHz, the baud rate generator needs a mod-163

(i.e., -i:;:::) counter, in which a one-clock-cycle tick is asserted once every 163 clock

cycles